PLEASE ENTER 6/12/06

In the Specification

Please replace the paragraph beginning at line 6 on page 4 with the following amended paragraph.

Write pre-compensation is a method to shift the write data timing in a direction to aid in pre-equalizing the signal. This optimizes the eventual readback signal; i.e., write signal modified based on prediction of what write signal will produce the cleanest readback signal using an understanding of physical/magnetic properties, i.e., predicting effects of distortion from ~~magnets~~ bits before/after that location before writing ~~a magnet~~ data on magnetic media. As ~~magnets~~ bits are written on a disk media, close ~~magnets~~ bits can partially erase each other as unwanted signal timing shift. Write pre-compensation can aid in fixing this problem. The media ~~magnets~~ bits may require substantial amounts of write pre-compensation based on adjacent ~~magnets~~ bits. Even if ~~magnets~~ bits are two or three ~~magnets~~ bits apart (1 0 0 1), the partial erasure influence could be significant enough to affect read back performance.

Please replace the paragraph beginning at line 10 on page 11 with the following amended paragraph.

Fig. 3 illustrates write pre-compensation 300 for the write data according to an embodiment of the present invention. Write pre-compensation is a method to shift the write data timing in a direction to aid in pre-equalizing the signal. As ~~magnets~~ bits are written on a disk media, close ~~magnets~~ bits can partially erase each other as unwanted signal timing shift. Write pre-compensation can aid in fixing this problem. Positive pre-compensation is defined as time shifting a pre-determined sequence of ~~magnets~~ bits in a positive direction relative to an isolated magnet. In Fig. 3, positive pre-compensation 310 and negative pre-compensation 320 is shown.

Please replace the paragraph beginning at line 3 on page 12 with the following amended paragraph.

Fig. 4 is a block diagram 400 of the write 410 and read 450 paths with write pre-compensation according to an embodiment of the present invention. The NRZI Write Data 412 is pre-compensated using read and write path circuitry. The read path 450 includes a first clock phase interpolator 452 that receives the coarse phase signals 404 from the ~~VCO~~ voltage-controlled oscillator (VCO) ring 402 and provides a clock signal 454 to the analog-to-digital converter 460. The analog-to-digital converter 460 provides a signal 462 to the read shift logic 470 to provide read phase select position signal 472 to the first clock phase interpolator 452. During a read operation the first clock phase interpolator 452 is used to track follow the data signal to provide synchronous clock and data to the data channel system using an A/D converter 460 and read shift logic 470. Thus, synchronous timing is provided by the first clock phase interpolator 452.

Please replace the paragraph beginning at line 7 on page 13 with the following amended paragraph.

Clock phase interpolators 452, 412 are used to generate different amounts of pre-compensation with adequate accuracy. As ~~magnets~~ bits are written on a disk media, close ~~magnets~~ bits can partially erase each other as unwanted signal timing shift. Write pre-compensation that provide one-length ~~magnet~~ bit pre-compensation amount of 0 to +/-30% with 1% to 2% accuracy may be required.